Bus system(Bus structure):-

The system bus connects the CPU (Processor), memory and peripherals devices (input/output device or secondary memory) with each other. The bus system carries data , address and control information . The speed of the system bus is the part of performance of computer system .

Note: The components of the computer system communicate with each other and with the outside world **through system bus. The processor connect to memory and peripheral devices by bus system.**

A Bus is a bunch of wires, and electrical path on the printed IC to which everything in the system is connected.

There are three types of Buses:

1- Address Buss (AB): is unidirectional (one direction) because address flow in one direction from processor to memory or from processor to input/ ouput devices .
The width of AB determines the amount of physical memory addressable by the processor.

2- Data Bus (DB): Is bidirectional (two direction) because allow data to transfer between the processor (Cpu) and memory (Ram).
the width of DB indicates the size of the data transferred between the processor and memory or I/O device.

3- Control Bus (CB): is bidirectional (two direction) used by cpu for communicating with other devices within the computer .It carries control signals from cpu and return status single from devices .The typical control signals ,include memory read, memory write, I/O read, I/O write, interrupt acknowledge, bus request.
These control signals indicates the type of action taking place in the computer system .

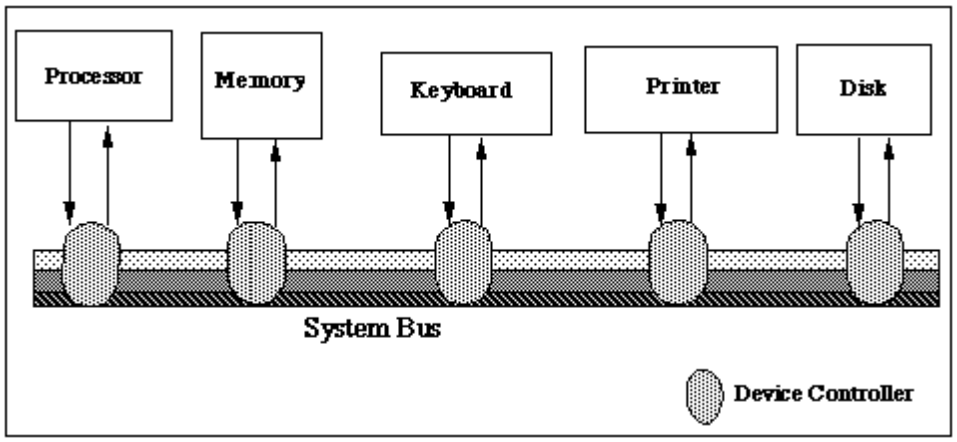


Figure1 (The system bus)

Memory (Main Memory)

The memory of a computer system consist of tiny electronics witches, with each switch set in one of two states: open or close.
It is however more convenient to think of these states **as 0 and 1**.Thus each switch can represent a binary digit or bit, as it is known, the memory unit consists of millions of such bits, bits are organized into groups of eight bits called **byte**. Memory can be viewed as consisting of an ordered sequence of bytes. Each byte in this memory can be identified by its sequence number starting with 0, as shown in Figure 2. This is referred to as memory

address of the byte. Such memory is called **byte addressable memory .**The memory address space of a system is determined by the address bus width of the CPU used in the system.

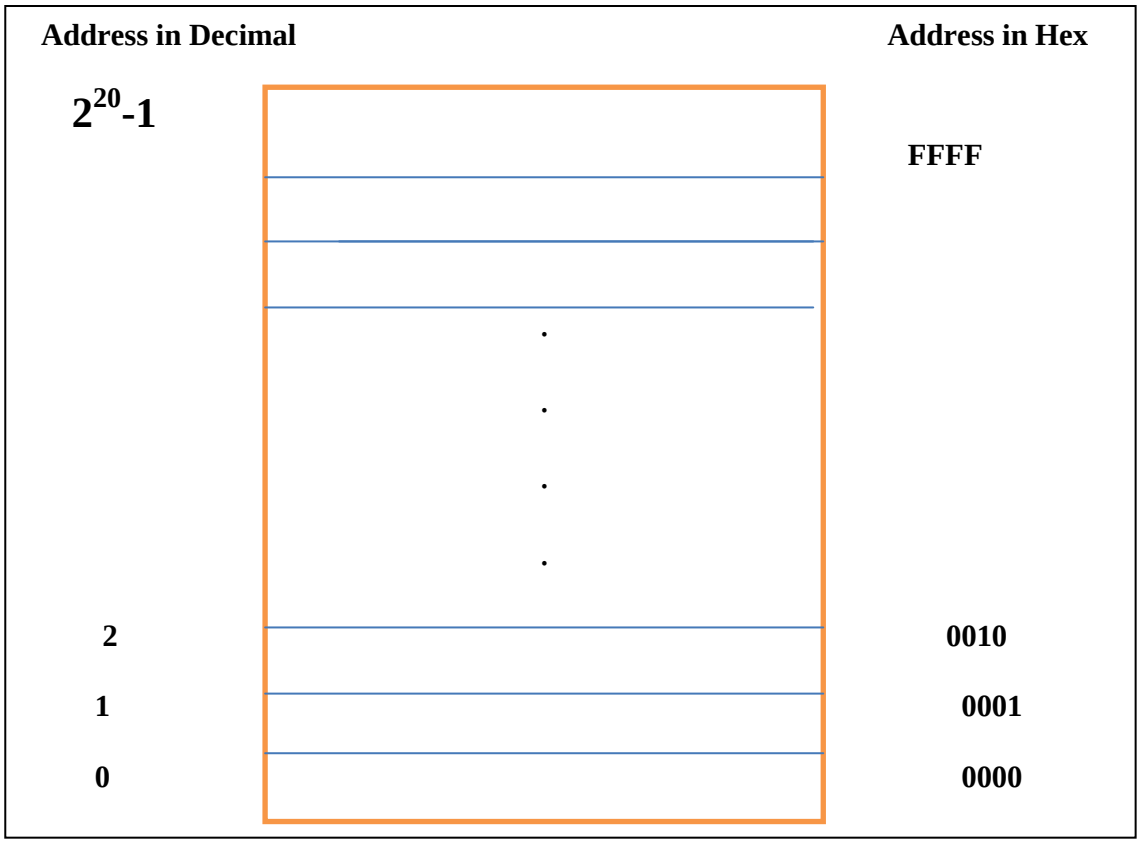


Figure 2: Logical view of the system memory

Two basic memory operations:-

The memory unit supports two fundamental operations: Read and Write . The read operation read a previously stored data and the write operation stores a value in memory.

Steps in a typical Read cycle:

1- Place the address of the location to be read on the address bus.
2- Activate the memory read control signal on the control bus.
3- Wait for the memory to retrieve the data from the address memory location.
4- Read the data from the data bus.
5- Drop the memory read control signal to terminate the read cycle.

Steps in a typical Write cycle:
1- Place the address of the location to be written on the address bus.
2- Place the data to be written on the data bus.
3- Activate the memory write control signal on the control bus.
4- Wait for the memory to store the data at the address location.
5- Drop the memory write control signal to terminate the write cycle.

Addresses: group of bits which are arranged sequentially in memory, to enable direct access, a number called address is associated with each group. Addresses start at 0 and increase for successive groups. The term location refers to a group of bits with a unique address. Table 1 represents Bit, Byte, and Larger units.

Table1: Bit, Byte, and Larger units.

Name	Number of Byte
Bit	0 or 1
Byte	is a group of bits used to represent a character, typically 8-bit.
Word	2-byte (16-bit)
Double Word	4-byte (32-bits)
Quad word	8-byte (64-byte)
Paragraph	16-byte (128-bit)
Kilo Byte (KB)	The number 210=1024=1 KB thus 640K=640*1024=655360 bytes)
Megabyte (MB)	(1024*1024) byte or 1,048,576 byte) approximately 1,000,000 bytes
Gigabyte (GB)	(1024*1024*10240byte) or (1,073,741,824 byte), approximately 1,000,000,000 bytes.
Terabyte (TB)	Approximately 1,000,000,000,000 bytes.

Memory chips:

Memory chips have two main properties that determine their application, storage capacity or size and access time or speed. A memory chip contains a number of locations, each of which stores one or more bits of data known as its bit width. The storage capacity of a memory chip is the product of the number of locations and the bit width. For example, a chip with 512 locations and a 2-bit data width has a memory size of 512×2=1024 bits.
Since the standard unit of data is a byte (8 bits), the above storage capacity is normally given as 1024/8 =128 bytes.
The number of locations may be obtained from the address width of the chip. For example, a chip with 10 address lines has 2^{10}= 1024 or 1 k locations. Given an 8-bit data width, a 10- bit address chip has a memory size of 2^{10} ×8 = 1024×8 = 1k ×1 byte = 1 KB.
The computer's word size can be expressed in bytes as well as in bits.

For example, a word size of 8-bit is also a word size of one byte; a word size of 16- bit is a word size of two byte. Computers are often described in terms of their word size, such as an 8-bit computer, a 16-bit computer and so on.
For example, a 16-bit computer is one in which the instruction data are stored in memory as 16-bit units, and processed by the CPU in 16-bit units. The word size also indicates the size of the data bus which carries data between the CPU and memory and between the CPU and I/O devices. To access the memory, to store or retrieve a single word of information, it is necessary to have a unique address.

The word address is the number that identifies the location of a word in a memory.
Each word stored in a memory device has a unique address. Addresses are always expressed as binary number, although hexadecimal and decimal numbers are often used for convenience.
The second properties of memory chips is access time, access time is the speed with which a location within the memory chip may be made a variable to the data bus. It is defend as the time interval between the instant that an address is sent to the memory chip and the instant that the data stored in to the location appears on the data bus. Access time is given in nanosecond (ns) and varies from 25 ns to the relatively slow 200 ns.

NOTS:

- The large computer(mainframes) have word-sizes that are usually in the 32-to-64 –bits range.

- Mini computers have a word sizes from 8-to-32-bits range.

- Microcomputers have a word sizes from 4-to-32-bits range.

In general a computer with a larger word size, can execute programs of instruction at a fast rate because more data and more instruction are stuffed into one word. The larger word sizes, however, mean more lines making up the data bus, and therefore more interconnections between the CPU and memory and I/O devices.
The word size is 4-bit therefore there are 4-data I/P lines and 4data O/P lines.
This memory has 32 different words, and therefore has 32 different
words, and therefore has 32 different addresses (storage location) from (00000) to(11111). Thus, we need a 5 address I/P lines.

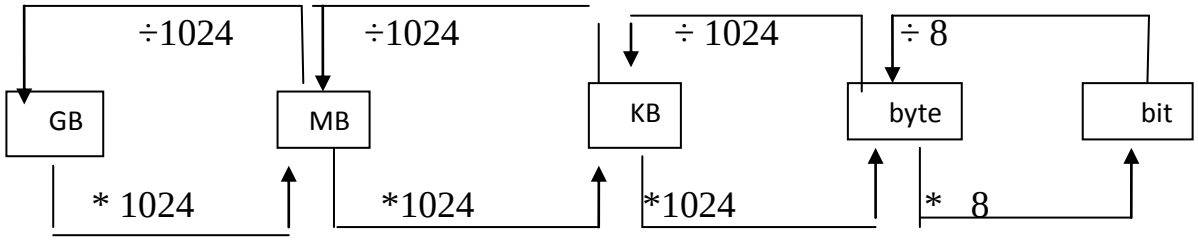
Memory capacity = number of memory storage
Location ×size of each word
= (number of word) × (number of bits per word)
= m (word)*n(bits)
= m*n bits

The capacity of memory depends on two parameters, the number of words (m) and the number of bits per word (n).
Every bit added to the length of address will double the number of words in the memory.
The increase in the number of bits per bits requires that an increase the length of data I/P and data O/P lines.

Memory capacity units

Byte ⟶ 8bits
KB ⟶ 1024 Byte
MB ⟶ 1024 KB
GB ⟶ 1024 MG
TB ⟶ 1024 GB

The following chat show the unit of memory capacity measurement .



ملاحظة : عندما نحول من الوحدة الكبيرة الى الصغيرة نقوم بالضرب في ١٠٢٤ ما عدا البايت الى البت نضربه فى ٨ وعلى ان تكون الوحدات متجاورة
اما من الصغير الي الكبير نقوم بالقسمة

EX: the capacity of memory is 2MG , what is the capacity in KB
2*1024= 2048 KB

EX: the capacity of memory is 10MG , what is the capacity in BYTE
10*1024 *1024 =10485760

EX: the capacity of memory is 2MG , what is the capacity in bit
2*1024*1024*8= 16777216 bits

EX: the capacity of memory is 16 bits , what is the capacity in Byte.
16/ 8 = 2 byte

EX: the capacity of memory is 20 KB , what is the capacity in MG.
20/ 1024=0.01953125 MG

EX: the capacity of memory is 15 KB , what is the capacity in GB
15/1024 /1024 = 0.0000143051 GB

Memory example

EX:-

A certain memory chip is specified as 2K×8:

1. How many words can be stored on this chip?
2. What is the words size?
3. How many total bits can this chip store?

SOL:-

1. 2K =2 × 1024 = 2048 words(bytes)
2. The word size is 8-bits (1 byte).
3. Capacity = 2048 × 8 = 16384 bits. Memory chip

EX:- A certain memory chip is specified as 2K × 16

1. How many words can be stored on this chip?
2. What is the words size?
3. How many total bits can this chip store?

SOL:-

1. 2K = 2 × 1024 = 2048 words(Bytes)
2. The word size is 16-bits(2 byte).
3. Capacity = 2048 * 16 = 32768 bits.

EX:- Which memory stores the most number of bits:
2MG × 8 memory or 2MG × 16 memory?

SOL:-

2MG= 2×1024× 1024 = 2 ×(1048576) =words

1. Capacity 2MG ×8 =(2 × 1024 ×1024) × 8 = 16,777,216 bits.
2. Capacity 2MG ×16=(2 × 1024 ×1024) ×16= 33,554,432 bits.

So 2MG × 16 memory is bigger than 2MG × 8

EX:- Which memory stores the most number of bits:
4MG × 8 memory or 2MG × 16 ?

SOL:-

1. Capacity = (4 × 1024 ×1024) × 8 =33,554,432 bits.
2. Capacity = (2 × 1024 × 1024) ×16= 33,554,432 bits.

EX:- A certain memory has a capacity of 4K × 8
1. How many data I/P & data O/P lines?
2. How many word address line?
3. What is its capacity in byte?

SOL:-

1. 8 each line: So data I/P lines = data O/P lines =8
2. 4 × 1024 = 4096 words

Thus, there are 4096 memory addresses

2^{12}=4096

so it required a 12 bit address line

3. The capacity = (4 ×1024) × 8= 32,768 bit = 32,769/8 =4096 byte (since 1byte = 8 bit).

EX: - the a certain memory has a capacity of 4K×16
1. How many data I/P & data O/P lines?
2. How many word address lines?
3. What is its capacity in byte?

SOL:-

1. 16 each one.

Data I/P lines = data O/P lines =16

2. 4 × 1024 = 4096 words

Thus, there are 4096 memory addresses.

$4096 = 2^{12}$

Its require a 12-bit address line.

3. Capacity = (4 × 1024) × 16 = 65,536 bit

= 65,536 / 8 = 8.192 byte

المحاضرة الثالثة

تقنيات الحاسبة

المرحلة الاولى