**Pipeline Hazards**

* Data Hazards – an instruction uses the result of the previous instruction. A hazard occurs exactly when an instruction tries to read a register in its ID stage that an earlier instruction intends to write in its WB stage.
* Control Hazards – the location of an instruction depends on previous instruction For example **Branch** instruction affects PC(program counter) contents .
* Structural Hazards – two instructions need to access the same resource

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**Stalling:**

* Stalling involves halting the flow of instructions until the required result is ready to be used. However stalling wastes processor time by doing nothing while waiting for the result.

