**MEMORY SYSTEM DESIGN USING ICs**

The major steps in such memory designs are the following:

1. Based on speed and cost parameters, determining the type of

memory ICs (static or dynamic) to be used in the design.

2. It is generally better to select an IC with the largest capacity in order to reduce the number of ICs in the system.

3. Determining the number of ICs needed

N = (total memory capacity)/( chip capacity).

4. Arranging the above N ICs in a P x Q matrix, where

Q = (number of bits per word in memory system)/(number of bits per word

in the IC) and P = N/Q.

5. Designing the decoding circuitry to select a unique word corresponding to each address.

The following examples illustrates the design:

***EX***: construct (64K x 16) memory using (16K x 1) memory chip:

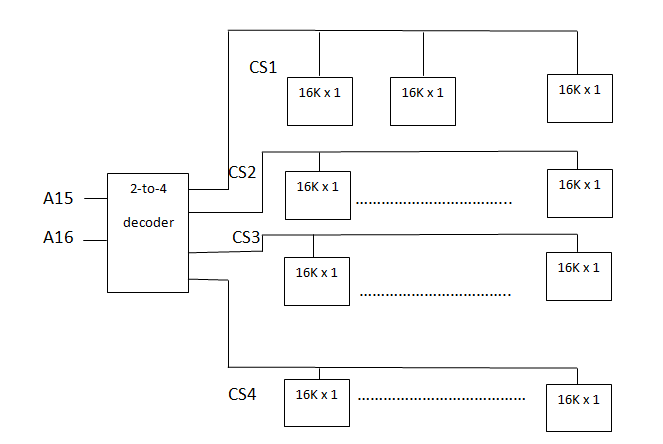
64K = 216 16 address line ( A1………A16)

16K= 214 14 address line (A1………A14)

We need 64 K/16 K = 4 row =P

We need 16/1= 16 column=Q

16-14=2 (A15 ,A16 ) we use them in a 2- to-4 decoder to select rows:



***EX***: construct (4K x 4) memory using (1K x 4) memory chip.

4K/1K = 4 row =P , 4/4=1 column =Q

4K= 212

1K= 210 12-10=2 then we use 2-to-4 decoder

