



**Ministry of Higher Education and Scientific Research**

**Mustansiriyah University / College of Science / Department of Computer Science**

**(الخطة الدراسية للمساق)**

**Course Plan**

**Course No.:** 50811210 **Time Division:** 3hr Theoretical and 2hr Practical

**Course Name:** Computer Architecture  **Semester & Year: Second, 2022 / 2023**

**Course Website:**

**Course Description:**

This course will describe the basics of modern processor operation. Topics include computer system performance, instruction set architectures, pipelining, branch prediction, memory-hierarchy design, and a brief introduction to multiprocessor architecture issues.

**This subject presents the** learn and understand of:

* Basic structure and operations of a computer.
* Arithmetic and logic unit and implementation of fixed-point and floating point arithmetic unit.
* Basics of pipelined execution.
* Parallelism and multi-core processors.
* Memory hierarchies, cache memories and virtual memories.
* Different ways of communication with I/O devices.

**Course Intended Outcomes:** Upon successful completion of the course, the student will be able to:

* Explain the importance of studying computer architecture.
* Evaluate various trades-offs while designing a computer system.
* Describe how various computer components interact in order to exchange information.
* Understanding the need for the use of memory hierarchy (cache, main memory, storage devices) to ensure the design of a balanced computer system.
* Describe how I/O systems work.
* Discuss the relationship between the design of a computer system and the design of an operating system to operate it.
* Describe the fundamental principles of CPU and control unit design.
* Evaluate various trade-offs in designing the instruction set architecture.
* Identify and evaluate various techniques for improving contemporary processor performance.

**Course Outline:**

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| **Week** | **Description depends on the Timing table (Theoretical)** | **Practical** |
| **1**  **1/3** | General Introduction & Review: Basic concepts revision, computer Architectures, computer design, History of computers, computer Components. | General Introduction of Emulator 8086 |
| **2**  **8/3** | Numbering System, Emulator 8086 instruction and instruction Types, General purpose registers | Numbering System |
| **3**  **15/3** | Combinational and sequential circuit :Multiplexers, Applications of Multiplexer, De-multiplexers, | assembly language (part1) |
| **4**  **22/3** | Basic of memory organization:, type of computer memory | assembly language (part2) |
| **5**  **29/3** | Main Memory Organization, location and Addressing Data | assembly language (part3) |
| **6**  **5/4** | Memory expansions, Instruction formats Addressing modes and effective address calculation. | 8086 interaction set1 |
| **7**  **12/4** | Central Processing: CPU Organization & Operation, Hardware Implementation: Bus and memory transfer, Micro operation, Arithmetic Logic Shift Unit. | 8086 interaction set2 |
| **8**  **19/4** | Exam1 | Exam 1 |
| **9**  **26/4** | Fundamental Concepts & Examples: CPU Organization According To Number of Buses, | Variables |
| **10**  **3/5** | Execute Of Complete Instruction, Design of Control Unit | Inside the CPU |
| **11**  **10/5** | Input-Output Organization: I/O interface, Microprocessor interface | Memory Access |
| **12**  **17/5** | Direct Memory Access: DMA example, I/O processor (IOP) | XCHG Instruction |
| **13**  **24/5** | Pipelining: instruction pipeline, RISC and CISC pipeline, SIMD processor | Arithmetic Instruction |
| **14**  **31/5** | Performance of Computer: Response time, throughput, CPU execution time, Basic Measurement Metrics, Performance Evaluation | Register Flag |
| **15**  **7/6** | Exam 2 | Exam 2 |

**Textbooks:**

**[1]:** Wang, Shuangbao Paul. *Computer Architecture and Organization: Fundamentals and Architecture Security*. Springer Nature, 2021.

**[2]:** Hwang, Kai, and Naresh Jotwani. *Advanced computer architecture, 3e*. McGraw-Hill Education, 2016.

**Suggested references:**

**[1]:** Harris, L. "Digital Design and Computer Architecture David M Harris & Sarah.",

**[2]:** Zomaya, Albert Y. "Advanced computer architecture and parallel processing." (2021)..

**Marking:**

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| --- | --- | --- | --- | --- |
| **Second Semester** | | | | **Final Exam** |
| **1st exam** | **2nd exam** | **Practical** | **Activity** |  |
| **10** | **10** | **14** | **6** | **60** |

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| **Assignment/ Project** | **Description** | **Due Date** | **Marking** |
| **test** | **written exam** | **/ /** |  |
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**Instructor(s) information [معلومات الأستاذ]**

1. **Section: (CS) ; Lecture Room:[302] , ; Office No.: ( 1)**

**Instructor's Name** (Practical): Samar Amil Kassir

**E-Mail**: **samarqassir@uomustansiriyah.edu.iq**

**Office Hours :**  **Tue.:[ 09 : 00 – 010: 40]**, **Thu.:[ 011 : 00 – 012: 40]**

**NOTES:**

**-Office Hour: Other office hours are available by appointment.**

**-The content of this syllabus not be changed during the current semester.**

**Lecturer Signature Chairman Signature**