Decoder and Encoder

Decoder:-

A decoder is a combinational logic circuit that converts coded information such as binary, into a recognizable form, such as decimal. There are many type of decoders such as:-

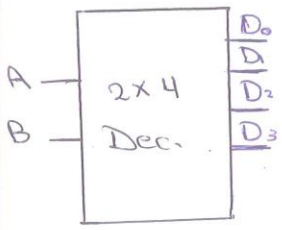
1- Binary decoder.
2- BCD to Decimal decoder.
3- BCD to 7-segment decoder.

Note:- In general form, a decoder has n input lines to handle n bits and form one to 2^n output lines to indicate the presence of one or more n-bit combinations.

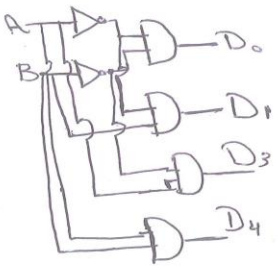
1- Binary decoder:- $(n*2^n)$ $(n\text{-to-}2^n)$ decoder.

It converts binary coded information in to adecimal recognizable form. The output lines of this decoder is 2^n where n is the number of bits of the binary input such as 2x4 decoder, 3x8 decoder, 4x16 decoder.

* 2x4 line decoder cct. is shown below with the Truth table



AB	D_0	D_1	D_2	D_3
0 0	1	0	0	0
0 1	0	1	0	0
1 0	0	0	1	0
1 1	0	0	0	1



From the truth table:-

$D_0 = \bar{A}\bar{B}$; $D_2 = A\bar{B}$

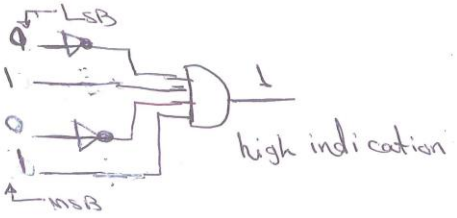
$D_1 = \bar{A}B$; $D_3 = AB$

Ex:- Show how you can indicat the No(10)16 for high or low
or Determine the logic required to decode the binary code 1010 with active high or low output.

Solution:- Active High

A AND gate is used and the output = 1

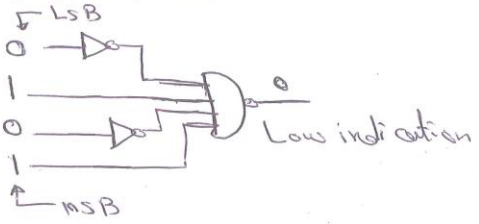
1010 = $A\bar{B}C\bar{D}$



Active Low

A NAND gate is used and the output = 0

1010 = $AB\bar{C}\bar{D}$



Implement Logic Functions Using Decoders:-

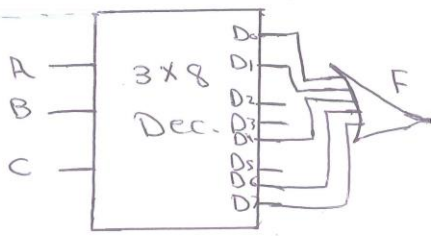
Ex:- Implement the following logic function using decoders and Logic gates:-

$F = \sum_{D_0\ D_1\ D_4\ D_6\ D_7} 0, 1, 4, 6, 7$

Solution:-

$D_0 = \bar{A}\bar{B}\bar{C}$
$D_1 = \bar{A}\bar{B}C$
$D_4 = A\bar{B}\bar{C}$
$D_6 = AB\bar{C}$
$D_7 = ABC$

ABC	F
000	1
001	1
010	0
011	1
100	0
101	1
110	1
111	1



$F = D_0 + D_1 + D_4 + D_6 + D_7$

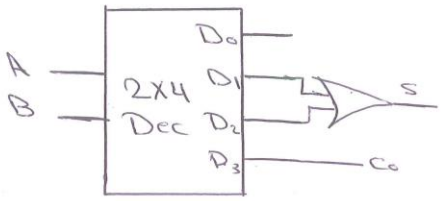
Ex:- Implement HA cct using decoder and logic gates:-

Solution:-

$S = \sum 1, 2 = \bar{A}B + A\bar{B} = D_1 + D_2$

$C_o = \sum 3 = AB = D_3$

AB	S	C_o
0 0	0	0
0 1	1	0
1 0	1	0
1 1	0	1



H.w:- By means of decoder and logic gates implement:-

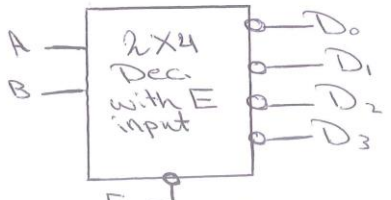
1- FA cct

2- $F = \sum o, 2, 5, 6, 7.$

Enable Control Inputs:-

Decoders include one or more enable inputs to control the circuit operation. In general, a decoder may operate with complemented or uncomplemented outputs. The enable inputs may be activated with a 0 or with a 1 signal. Some decoders have two or more enable i/p's that must satisfy a given logic condition in order to enable the cct.

A 2X4 line decoder with an enable input constructed with NAND gate is shown below:-



2-to-4 Decoder with Enable input (Active Low)

E_o	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

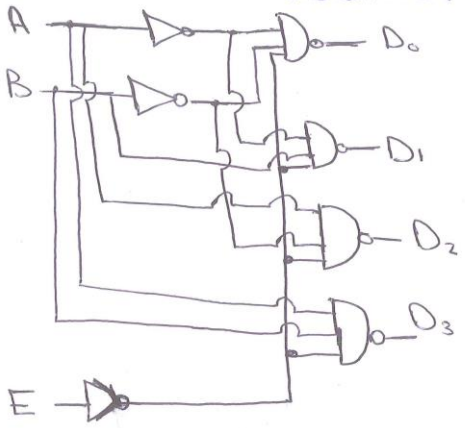
Truth Table

$D_0 = \overline{\bar{E}\bar{A}\bar{B}}$

$D_1 = \overline{\bar{E}\bar{A}B}$

$D_3 = \overline{\bar{E}AB}$

$D_4 = \overline{EAB}$



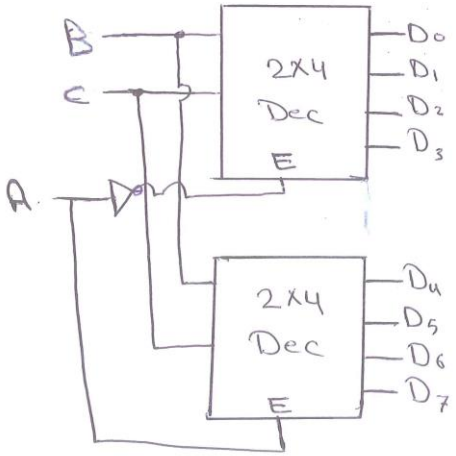
VLP

Note:- Decoders with enable inputs can be connected together to form a larger decoder circuit.

Ex:- Design 3×8 decoder using 2×4 decoders with Enable:-

Solution:-

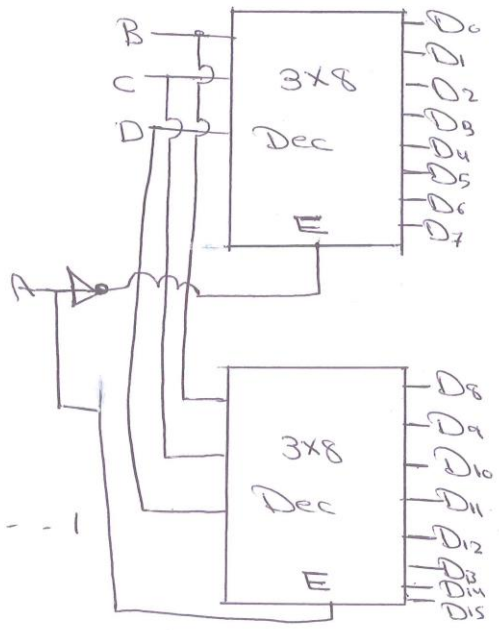
	A B C	D_0 D_1 D_2 .... D_7
1st Dec	0 0 0	1 0 0 - - - 0
	0 0 1	0 1 0 - - - 0
	0 1 0	0 0 1 - - - - 0
	0 1 1	.
		.
2nd Dec	1 0 0	.
	1 0 1	.
	1 1 0	.
	1 1 1	0 0 0 - - - 1



Ex:- Design 4 to-16 Decoder, using 3×8 decoders with enable.

Solution:-

	A	B	C	D	D_0	D_1	...	D_{15}
1st Dec	0	0	0	0	1	0	...	0
	0	0	0	1	0	1	...	0
	0	0	1	0				
	0	0	1	1				
	0	1	0	0				
	0	1	0	1				
	0	1	1	0				
	0	1	1	1				
2nd Dec	1	0	0	0				
	1	0	0	1				
	1	0	1	0				
	1	0	1	1				
	1	1	0	0				
	1	1	0	1				
	1	1	1	0				
	1	1	1	1	0	0	...	1



H.W:- Design 4-to-16 Decoder, using 2X4 decoders with enables.