Excitation Tables

During the design process we usually know the transition from the present state to next state and wish to find the flip-flop input conditions that will cause the required transition. For this reason, we need a table that lists the required inputs for a given change of state. Such a table is called an excitation table.

When D type flip-flops are employed, the input equations are obtained directly from the next state. This is not the case for the **JK** and **T** types of flip-flops.

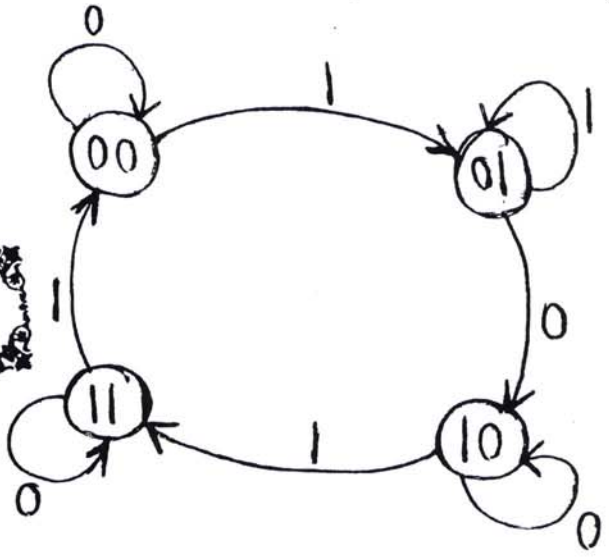
The excitation tables for the JK and T flip-flops are shown below:

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

X represents don't-care condition, which means that it does not matter whether the input is 1 or 0.

Ex: Synthesize (Design) the sequential circuit ~~that~~ specified by the following state diagram, using JK flip-flops.



Soln

Present state		i/p	Next state		Flip-Flop inputs			
A	B	X	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

The next-state values are not used during the simplification since the input equations are a function of the present state and input only.

A \ Bx	00	01	11	10
0				1
1	X	X	X	X

$J_A = B\bar{x}$

A \ Bx	00	01	11	10
0	X	X	X	X
1			1	

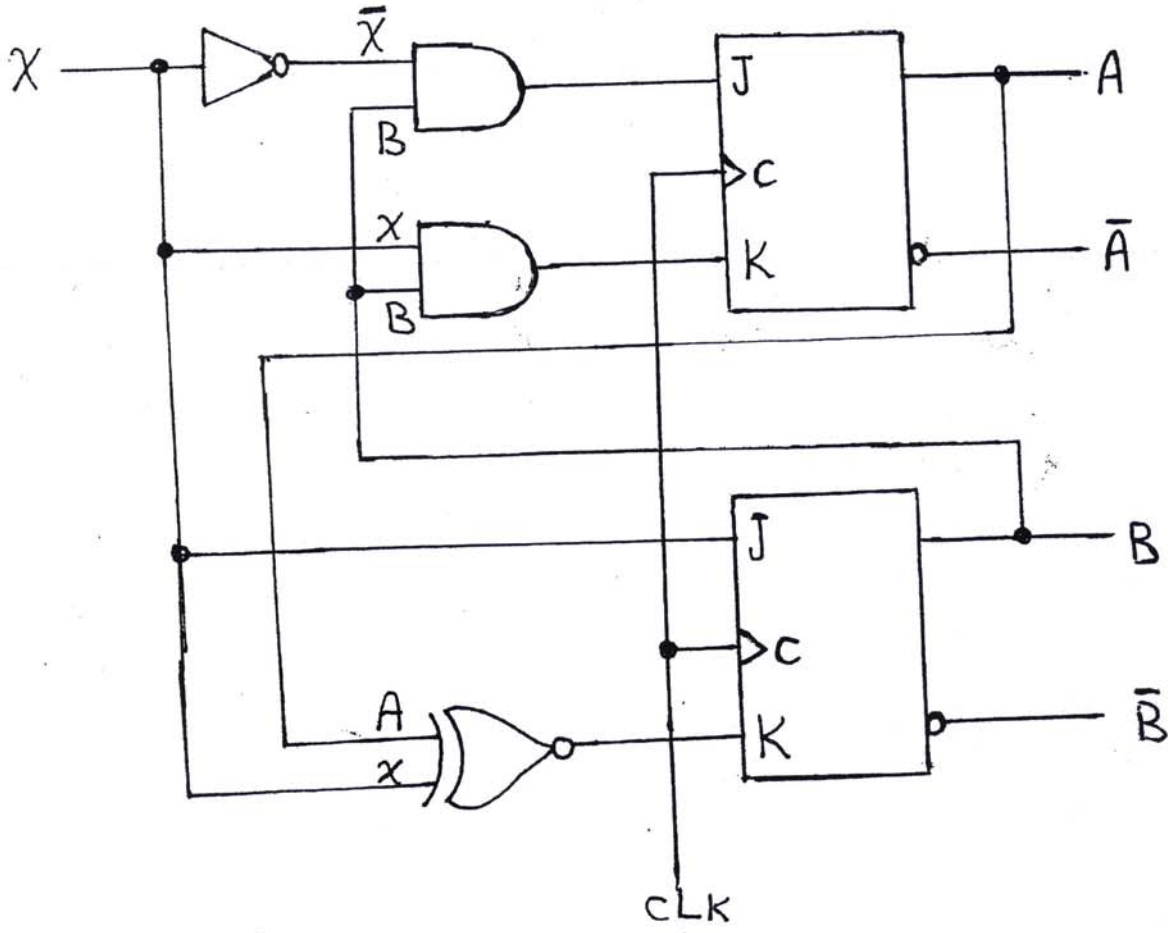
$K_A = Bx$

A \ Bx	00	01	11	10
0		1	X	X
1		1	X	X

$J_B = x$

A \ Bx	00	01	11	10
0	X	X		1
1	X	X	1	

$K_B = \overline{(A \oplus x)}$



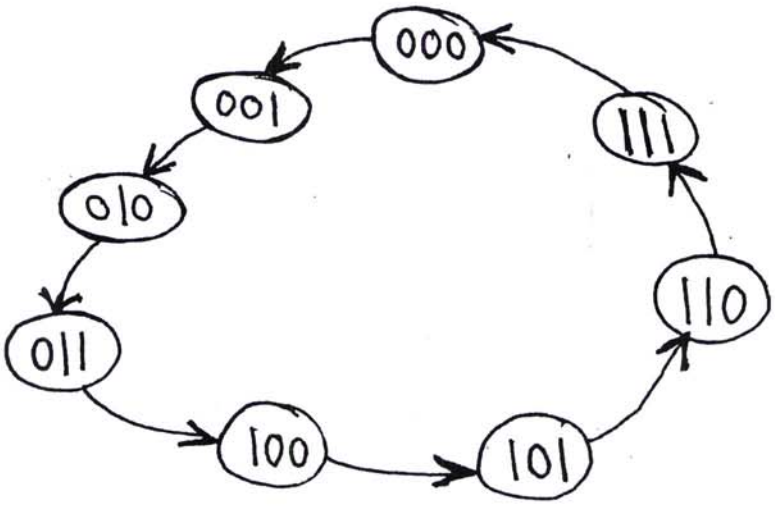
The Binary Counter

An n-bit binary counter consists of n flip-flops that can count in binary from 0 to $2^n - 1$. The flip-flop output repeat the binary count sequence with a return to 000 after 111. The state transitions in clocked sequential circuits occure during a clock edge; the flip-flops remain in their present states if no clock is applied. For this reason, the clock does not appear explicitly as an input variable in a state diagram or state table.

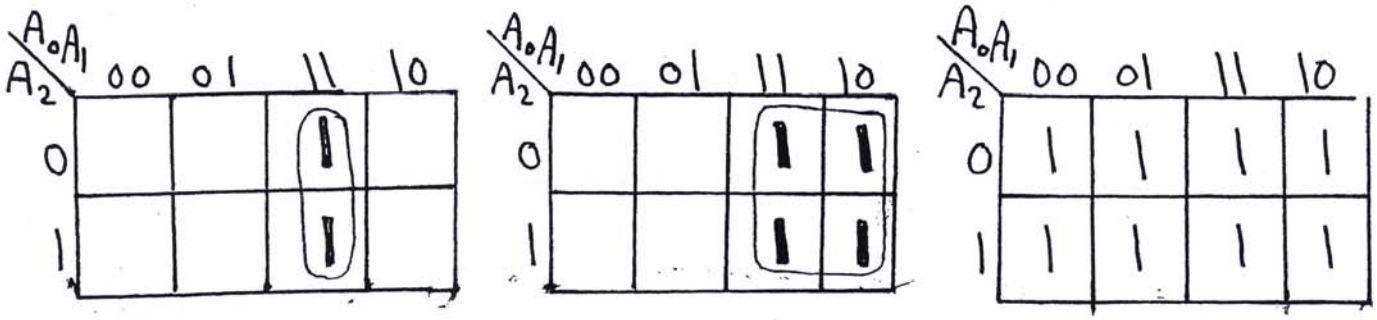
From this point of view, the state diagram of a counter does not have to show input and output values along the directed lines. The only input to the circuit is the clock, and the outputs are specified by the present state of the flip-flops.

Ex: Design a 3-bit binary counter using T flip-flops.

Soln: The 3-bit counter state diagram is:



Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A_2}	T_{A_1}	T_{A_0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



$T_{A_2} = A_1 A_0$ $\quad$ $T_{A_1} = A_0$ $\quad$ $T_{A_0} = 1$