State Reduction and Assignment

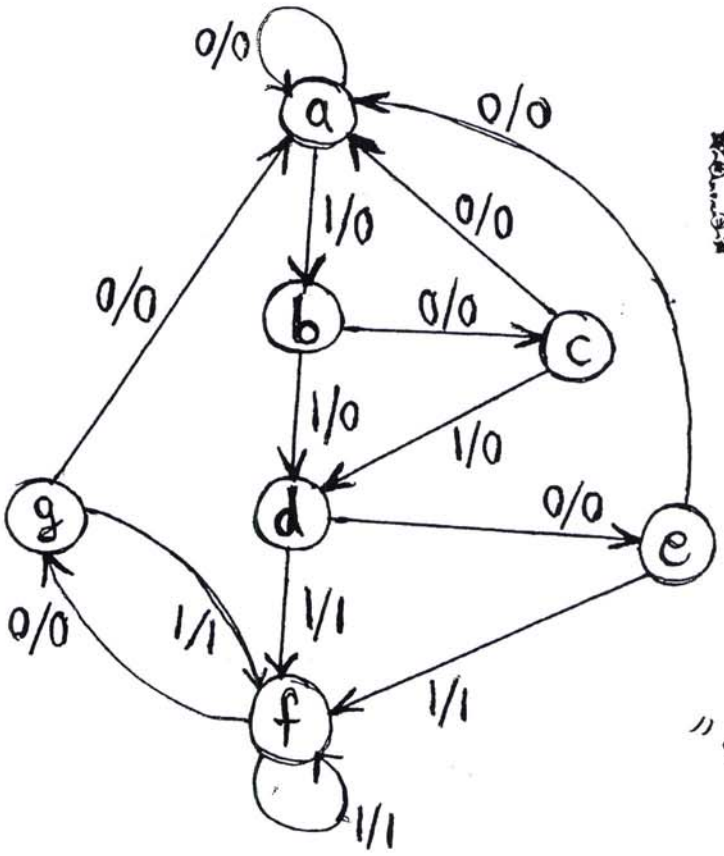
The analysis of sequential circuits starts from a circuit diagram and culminates in a state table or diagram. The design of a sequential circuits starts from a set of specifications and culminates in a logic diagram.

State Reduction

The reduction of the number of flip-flops in a sequential circuit is referred to as the state reduction problem. State reduction algorithms are concerned with procedures for reducing the number of states in a state table, while keeping the external input-output requirments unchanged. Since m flip-flops produce 2^m state, a reduction in the number of states may (or may not) result in a reduction in the number of flip-flops. An unpredictable effect in reducing the number of flip-flops is that sometimes the equivalent circuit (with fewer flip-flops) may require more combinational gates

Ex: Reduce the following state diagram to a minimum number of state:

Soln: We need the state table, it is listed in the next Page and it is obtained directly from the state diagram



"state diagram"

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Algorithm: Two states are said to be equivalent if, for each member of the set of inputs, they give exact the same output and send the circuit either to the same state or to an equivalent state.

When two states are equivalent, one of them can be removed without altering the input-output relationships.

States g and e go to states a and f and have outputs 0 and 1 for $X=0$ and $X=1$, therefore, they are equivalent and one of these states can be removed.

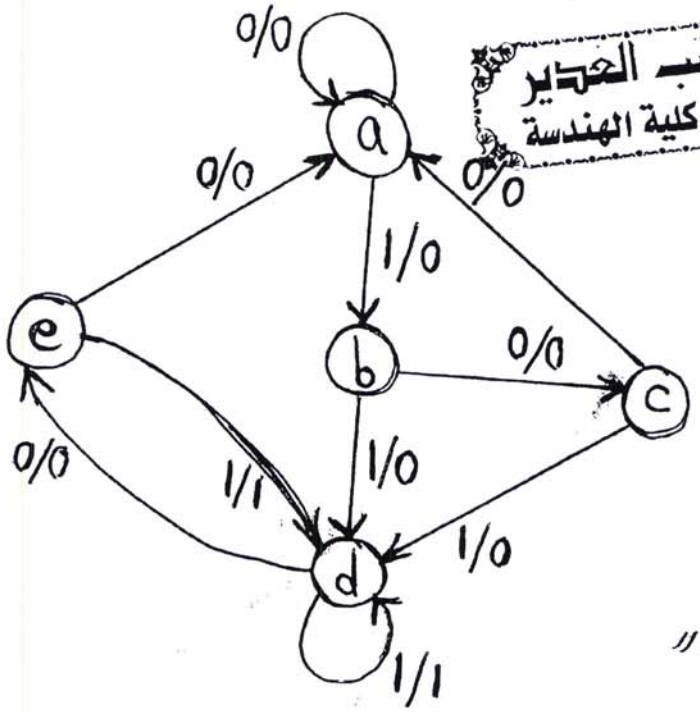
The raw with present state g is removed and state g is replaced by state e each time it occurs in the next-state columns.

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

States f and d are also equivalent and state f can be removed and replaced by d.

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

The sequential circuit was reduced from 7 to 5 states, and still satisfies the original input-output specifications



"Reduced state diagram

In fact, this state diagram is exactly the same as that at the begining.

State Assignment

In order to design a sequential circuit with physical components, it is necessary to assign coded binary values to the states. For a circuit with m states, the codes must contain n bits where $2^n \geq m$. For example with three bits it is possible to assign codes to eight states denoted by binary numbers 000 through 111.

The binary form of the state table is used to derive the combinational circuit part of the sequential circuit.

Design Procedure

The design of a clocked sequential circuit starts from a set of specifications and culminates in a logic diagram or a list of Boolean functions from which the logic diagram can be obtained. The first step in the design of sequential circuits is to obtain a state table or an equivalent representation, such as a state diagram.

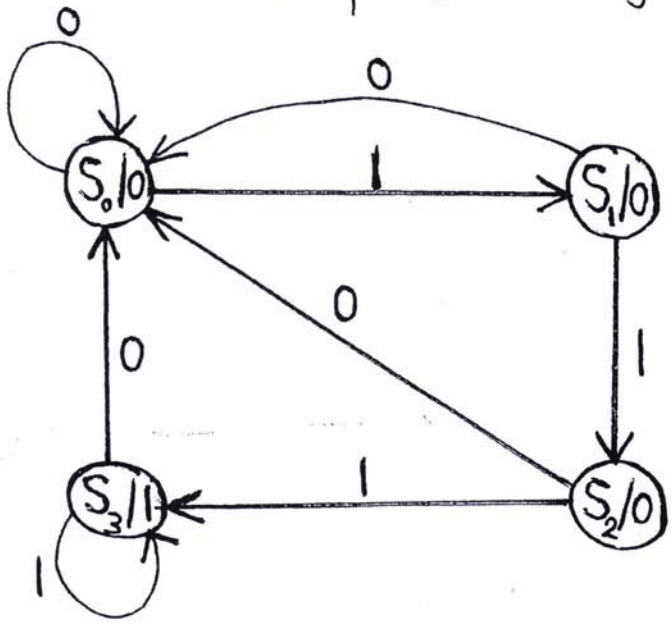
A synchronous sequential circuit is made up of flip-flops and combinational gates. The number of flip-flops is determined from the number of states needed in the circuit. The combinational circuit is derived from the state table by evaluating the flip-flop input equations and output equations.

The procedure for designing synchronous sequential circuits can be summarized by a list of recommended steps.

1- From the word description and specifications of the desired operation, derive a state diagram for the circuit.
2- Reduce the number of states if necessary.
3- Assign binary values to the states.
4- Obtain the binary-coded state table.
5- Choose the type of flip-flops to be used.
6- Derive the simplified flip-flop input equations and output equations.
7- Draw the logic diagram.

Ex: Design a circuit that detects three or more consecutive 1's in a string of bits coming through an input line, using D flip-flops. (Moore system)

Soln: The first step is, drawing the state diagram.



A B
$S_0 = 0\ 0$
$S_1 = 0\ 1$
$S_2 = 1\ 0$
$S_3 = 1\ 1$

input is x
output is y

Present state A	Present state B	i/p x	Next state A	Next state B	o/p y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

The char. eqn. of the D flip-flop is

$Q(t+1) = D_Q$

$A(t+1) = D_A(A,B,x)$

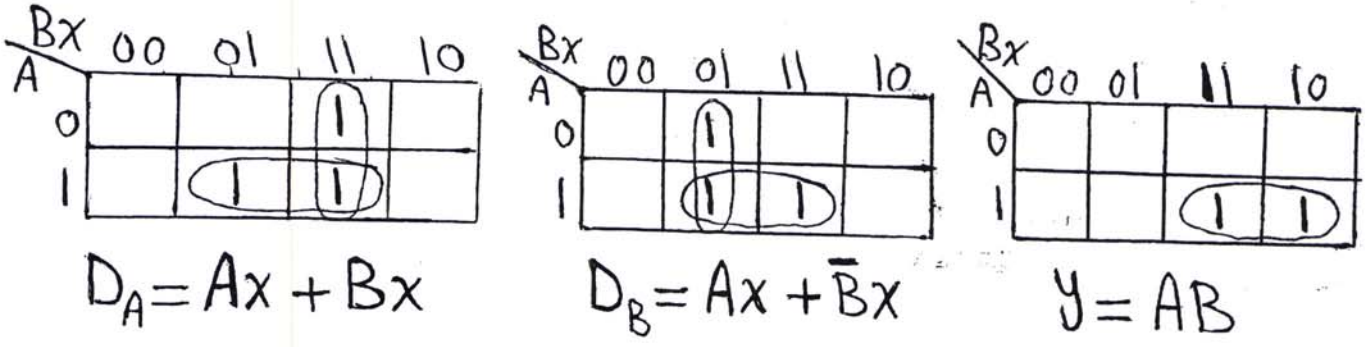
$A(t+1) = \Sigma(3,5,7)$

$B(t+1) = D_B(A,B,x)$

$B(t+1) = \Sigma(1,5,7)$

$y(A,B,x) = \Sigma(6,7)$

Where A and B are the present-state values of flip-flops A and B, x is the input, and D_A and D_B are the input equations.



$D_A = Ax + Bx$ $D_B = Ax + \bar{B}x$ $y = AB$