the binary information that was present at the data input at the time the transition occured is retained at the Q output until the control input is enabled again.

# Flip-Flops

A flip-flop is a clocked binary storage device, that is, a device that stores either a 0 or a 1. The state of the system (that is, what is in memory) changes on the transition of the clock. For some flip flops, that change takes place when the clock goes from 1 to 0; that is referred to as trailing-edge triggered. For others, that changes takes place when the clock goes from 0 to 1; that is referred to as leading-edge triggered.

trailing

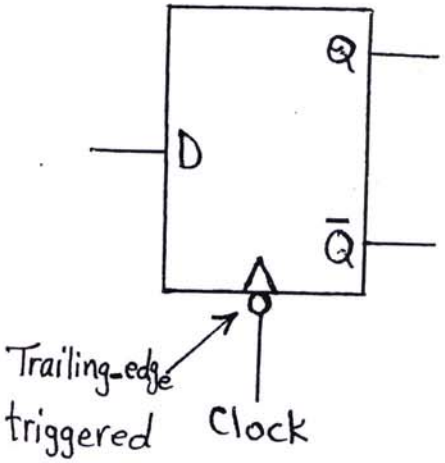
leading

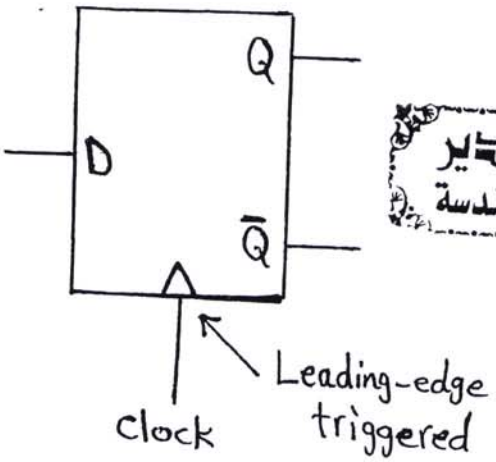
Flip flops have one or two outputs. One output is the state of the flip flop. If there are two, the other output is the complement of the state.

## D flip-flop

The simplest flip flop is the D flip flop. The name comes from Delay, since the output is just the input delayed until the next active clock transition. The next state of the D flip flop is the value of D before the clock transition.

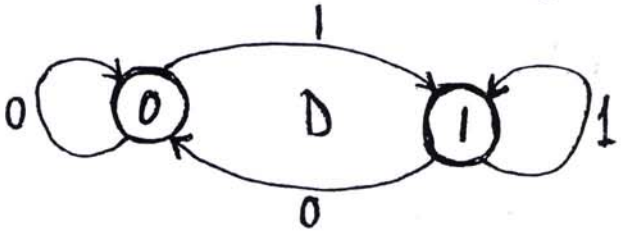
"D flip-flop diagrams"






"State diagram"

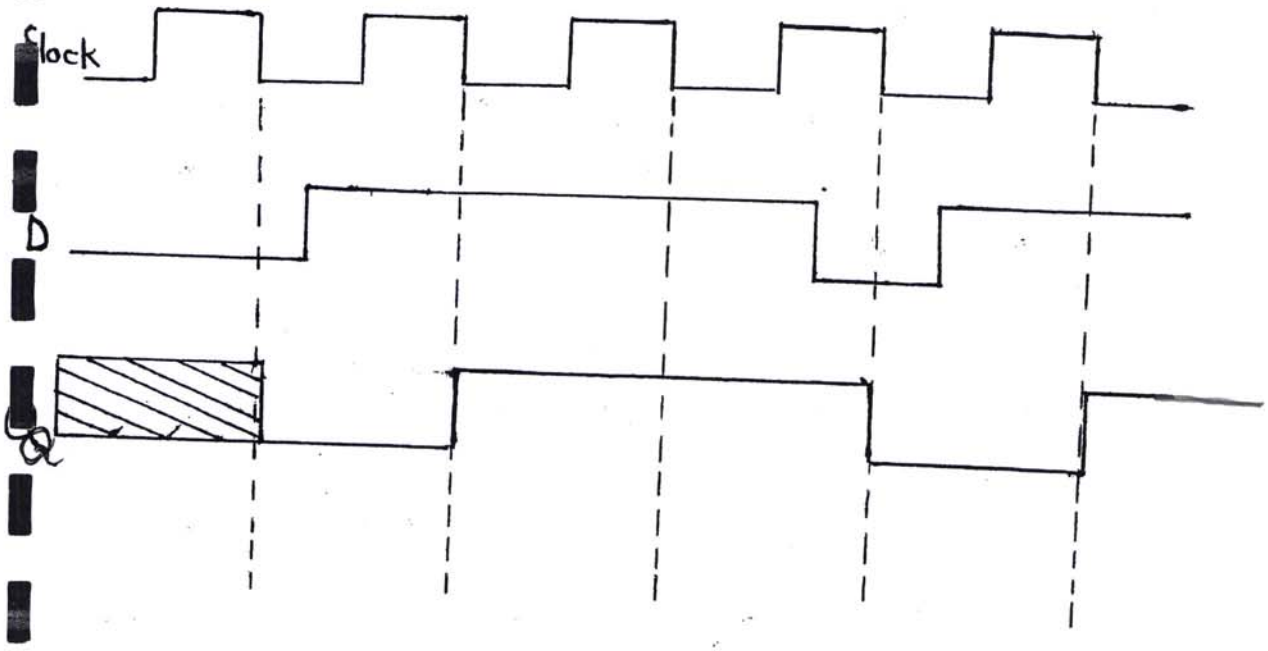



"Truth table"

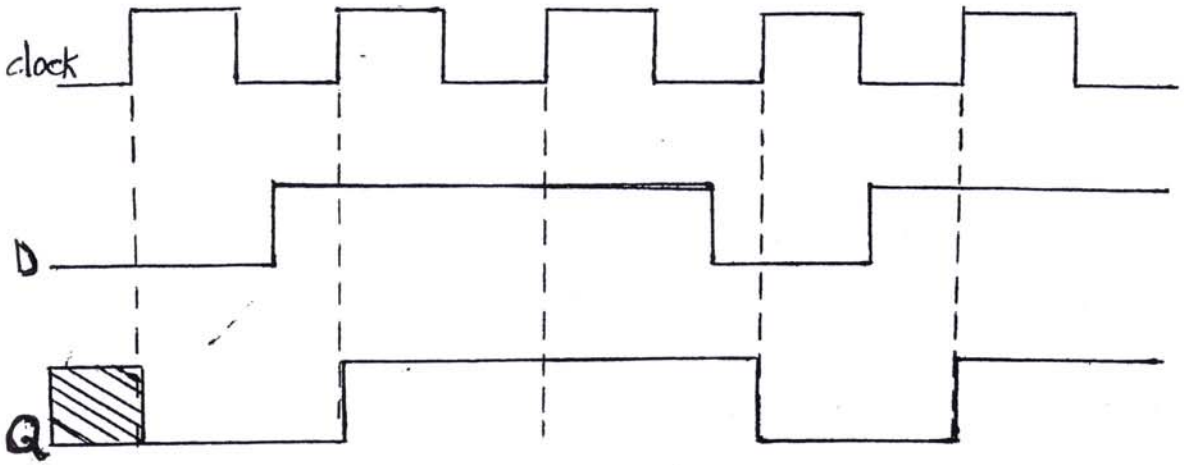
| D | Q(t+1) | |
|---|---|---|
| 0 | 0 | Reset |
| 1 | 1 | Set |

Char. eqn. $Q(t+1) = D$

The behaviour of a trailing-edge triggered D flip flop is illustrated in the following timing diagram.



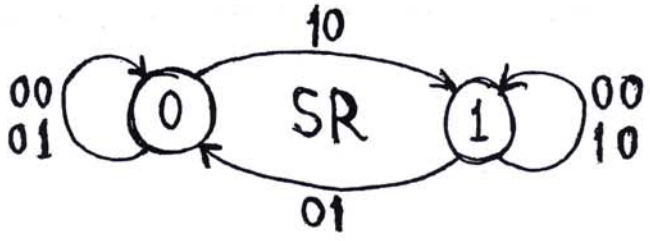
A timing diagram for a leading-edge triggered D flip flop, using the same input as before, is shown below.

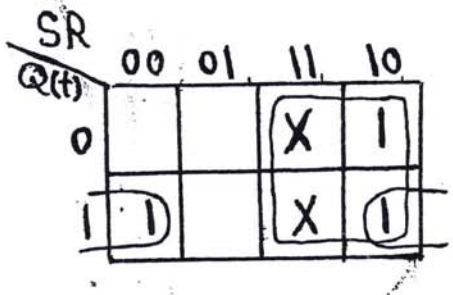



## SR Flip-Flop

The SR (Set-Reset) flip flop has two inputs, S and R, which have the same meaning as those for the SR latch. Its behavior is described by the truth table below and state diagram.

| S | R | Q(t+1) |
|---|---|---|
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | – not allowed |



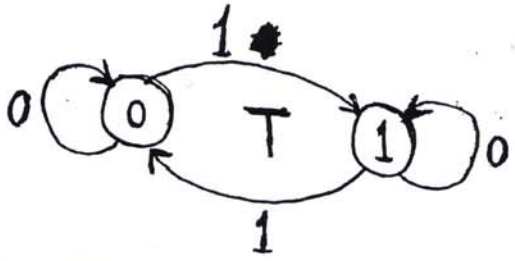

char. eqn.

$$Q(t+1) = S + \bar{R}\,Q(t)$$

# T Flip-Flop

The T (Toggle) flip flop has one input, T, such that if T=1, the flip flop changes state (that is, is toggled), and if T=0, the state remains the same. The truth table describing the behavior of the T flip flop and the state diagram are shown below.

| T | Q(t+1) | |
|---|---|---|
| 0 | Q(t) | No change |
| 1 | $\bar{Q}(t)$ | Complement |



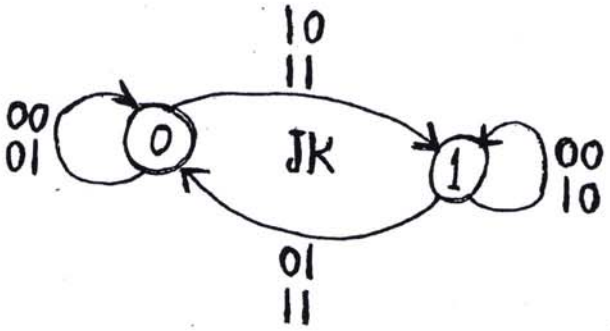

The behavioral equation is:

$$Q(t+1) = T \oplus Q(t)$$
$$Q(t+1) = T\bar{Q} + \bar{T}Q$$

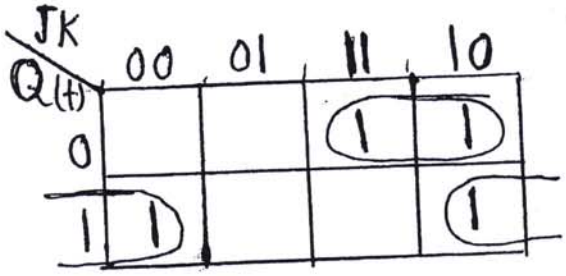
# JK Flip-Flop

It is a combination of the SR and T, in that it behaves like an SR flip flop, except that J=K=1 causes the flip flop to change states (as in T=1). The truth table and state diagram are shown below.

| J | K | Q(t+1) | |
|---|---|---|---|
| 0 | 0 | Q(t) | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | $\bar{Q}(t)$ | Complement |



from the truth table, we can derive the following map and the equation for Q(t+1).




$$Q(t+1) = J\bar{Q}(t) + \bar{K}Q(t)$$

char. eqn.

The 7473 is a dual JK flipflop package, active low clear input, ~~trailing~~ trailing-edge triggered, two outputs Q and $\bar{Q}$, 14 pin IC.

The 7474 is a dual D flip flop, 14-pin package, leading--edge triggered, active low preset inputs.

There are packages of D flip flops with four or six flip flops. The 74174 is a hex (six) D flip flop package, with only a Q output for each flip flop and a common leading-edge triggered clock. There is a common active low clear (Master Reset). This is a 16-pin package.

The 74175 a quad (four) D flip flop package. Each flip flop has both a Q and $\bar{Q}$ output. There is a common leading-edge triggered clock and a common active low clear. It is a 16-pin package.